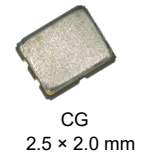
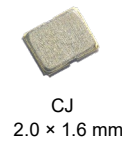


CRYSTAL OSCILLATOR (Programmable)
OUTPUT: CMOS

Product Number
SG-8201CJ: X1G005981xxxx16
SG-8201CG: X1G006191xxxx16

SG-8201 series

- Frequency range : 1.2 MHz to 170 MHz
- Supply voltage : 1.62 V to 3.63 V
- Function : Output enable (OE/ \overline{OE}) or Standby (\overline{ST} / \overline{ST})
- Frequency tolerance, operating temperature:
 - $\pm 15 \times 10^{-6}$ (-40 °C to +105 °C)
 - $\pm 25 \times 10^{-6}$ (-40 °C to +125 °C)
- PLL technology to enable setting any output frequency



Specifications (characteristics)

Item	Symbol	Specifications			Conditions/Remarks			
		1.80 V Typ. 1.62 V to 1.98 V	2.50 V Typ. 2.25 V to 2.75 V	3.30 V Typ. 2.97 V to 3.63 V				
Supply voltage	V_{CC}							
Output frequency range	f_o	1.2 MHz to 170 MHz						
Storage temperature range	T_{stg}	-55 °C to +125 °C			Storage as single product.			
Operating temperature range	T_{use}	H: -40 °C to +105 °C J: -40 °C to +125 °C						
Frequency tolerance ^{*1}	f_{tol}	B: $\pm 15 \times 10^{-6}$			$T_{use} = -40 \text{ °C to } +105 \text{ °C}$			
		D: $\pm 25 \times 10^{-6}$			$T_{use} = -40 \text{ °C to } +125 \text{ °C}$			
Current consumption	I_{CC}	5.2 mA Typ.	5.4 mA Typ.	5.6 mA Typ.	1.2 MHz $\leq f_o \leq$ 25 MHz	No load, Rise/Fall time: Default		
		7.0 mA Max.	7.2 mA Max.	7.5 mA Max.			25 MHz $< f_o \leq$ 50 MHz	
		5.4 mA Typ.	5.7 mA Typ.	6.1 mA Typ.	50 MHz $< f_o \leq$ 75 MHz			
		7.3 mA Max.	7.6 mA Max.	8.1 mA Max.			75 MHz $< f_o \leq$ 100 MHz	
		5.7 mA Typ.	6.3 mA Typ.	7.0 mA Typ.	100 MHz $< f_o \leq$ 125 MHz			
		7.7 mA Max.	8.2 mA Max.	9.1 mA Max.			125 MHz $< f_o \leq$ 170 MHz	
		6.2 mA Typ.	6.9 mA Typ.	7.9 mA Typ.				
		8.2 mA Max.	9.1 mA Max.	10.4 mA Max.				
		6.9 mA Typ.	7.9 mA Typ.	9.1 mA Typ.				
		9.4 mA Max.	10.7 mA Max.	12.4 mA Max.				
Output disable current	I_{dis}	5.0 mA Typ.	5.0 mA Typ.	5.1 mA Typ.	OE = GND, $\overline{OE} = V_{CC}$			
		7.2 mA Max.	7.3 mA Max.	7.4 mA Max.				
Standby current	I_{std}	0.3 μ A Typ.	0.3 μ A Typ.	0.5 μ A Typ.	ST = GND, ST = V_{CC}			
		15.0 μ A Max.	15.0 μ A Max.	15.0 μ A Max.				
Symmetry	SYM	45 % to 55 %			50 % V_{CC} Level, $L_{CMOS} \leq 15$ pF			
Output voltage (DC characteristics)	V_{OH}	90 % V_{CC} Min.			Rise/Fall time			
					Default 'A' Option ^{*2}	Other Options	I_{OH}	I_{OL}
	V_{OL}	10 % V_{CC} Max.			fo > 125 MHz	B: Faster	-2.0 mA	2.0 mA
					75 MHz $< f_o \leq$ 125 MHz	C: Fast	-1.0 mA	1.0 mA
					50 MHz $< f_o \leq$ 75 MHz	D: Slow	-0.5 mA	0.5 mA
			fo \leq 50 MHz	E: Slower	-0.2 mA	0.2 mA		
Output load condition	L_{CMOS}	15 pF Max.						
Input voltage	V_{IH}	70 % V_{CC} Min.			Pin 1			
	V_{IL}	30 % V_{CC} Max.						
Rise/Fall time	tr/ff	-			Default 'A' Option ^{*2}	Other Options	20 % - 80 % V_{CC} , $L_{CMOS} = 15$ pF	
		2.0 ns Max.			fo > 125 MHz	B: Faster		
		2.5 ns Max.			75 MHz $< f_o \leq$ 125 MHz	C: Fast		
		4.0 ns Max.			50 MHz $< f_o \leq$ 75 MHz	D: Slow		
6.0 ns Max.			fo \leq 50 MHz	E: Slower				
Output disable time (OE)	tstp_oe	1 μ s Max.			Measured from the time OE or \overline{ST} pin crosses 30 % V_{CC} or measured from the time \overline{OE} or ST pin crosses 70 % V_{CC}			
Output disable time (ST)	tstp_st							
Output enable time (OE)	tsta_oe	100 ns + 2 clock cycle Max.			Measured from the time OE pin crosses 70 % V_{CC} or measured from the time \overline{OE} pin crosses 30 % V_{CC}			
Output enable time (ST)	tsta_st	3 ms Max.			Measured from the time \overline{ST} pin crosses 70 % V_{CC} or measured from the time ST pin crosses 30 % V_{CC}			
Start-up time	t_str	3 ms Max.			Measured from the time V_{CC} reaches its rated minimum value, 1.62 V			
Phase Jitter	t_{PJ}	1.2 ps Typ.			fo = 25 MHz, Offset frequency: 12 kHz to 5 MHz			
		1.2 ps Typ.			fo = 50 MHz, Offset frequency: 12 kHz to 20 MHz			
		1.2 ps Typ.			fo = 75 MHz, Offset frequency: 12 kHz to 20 MHz			
		1.2 ps Typ.			fo = 100 MHz, Offset frequency: 12 kHz to 20 MHz			
		1.1 ps Typ.			fo = 125 MHz, Offset frequency: 12 kHz to 20 MHz			
		1.4 ps Typ.			fo = 150 MHz, Offset frequency: 12 kHz to 20 MHz			
1.5 ps Typ.			fo = 170 MHz, Offset frequency: 12 kHz to 20 MHz					
Frequency aging	f_{age}	This is included in frequency tolerance specification.			+25 °C, first year			

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage variation, reflow drift, load drift and aging (+25 °C, 1 year).

*2 Default 'A' Rise/Fall time and I_{OH}/I_{OL} are dependent on programmed frequency.

Pin description

Pin	Name	I/O type	Function	
1	OE	Input	Output Enable	High ^{*1} or Open: Specified frequency output from OUT pin Low: OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	\overline{OE}	Input	Output Enable	Low ^{*2} or Open: Specified frequency output from OUT pin High: OUT pin is low (pull down with 500 kΩ), only output driver is disabled.
	\overline{ST}	Input	Standby	High ^{*1*3} : Specified frequency output from OUT pin Low: OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I _{std} .
	ST	Input	Standby	Low ^{*2*3} : Specified frequency output from OUT pin High: OUT pin is low (pull down with 500 kΩ), Device goes to standby mode. Supply current reduces to the least as I _{std} .
2	GND	Power	Ground	
3	OUT	Output	Clock output	
4	V _{CC}	Power	Power supply	

*1 If fixing it at High, please connect to V_{CC} directly.
 *2 If fixing it at Low, please connect to GND directly.
 *3 If necessary to use Open, please select Output Enable function.

Product Name

SG-8201CJ 170.000000MHz T D J P A
 a b c d e f g h

b: Package type	
CJ	2.0 mm × 1.6 mm
CG	2.5 mm × 2.0 mm

e: Frequency tolerance / f: Operating temperature	
BH	±15 × 10 ⁻⁶ / -40 °C to +105 °C
DJ	±25 × 10 ⁻⁶ / -40 °C to +125 °C

a: Model b: Package type
 c: Frequency d: Supply voltage (T: 1.8 V to 3.3 V Typ.)
 e: Frequency tolerance f: Operating temperature
 g: Function h: Rise/Fall time

g: Function	
P	Output Enable (OE)
Q	Output Enable (\overline{OE})
S	Standby (\overline{ST})
T	Standby (ST)

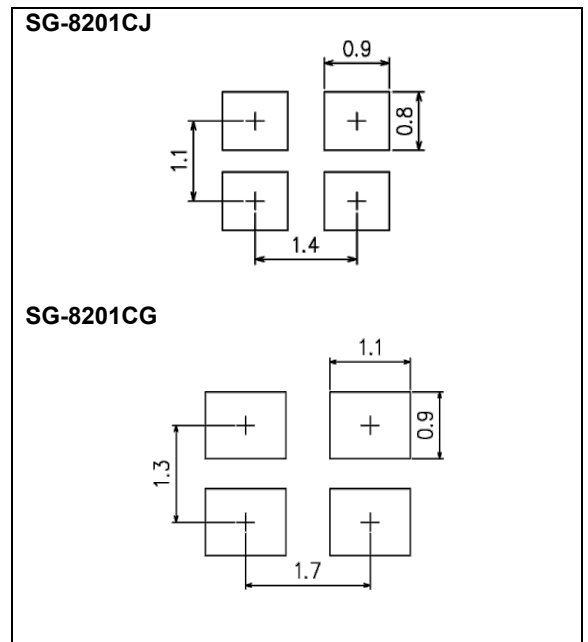
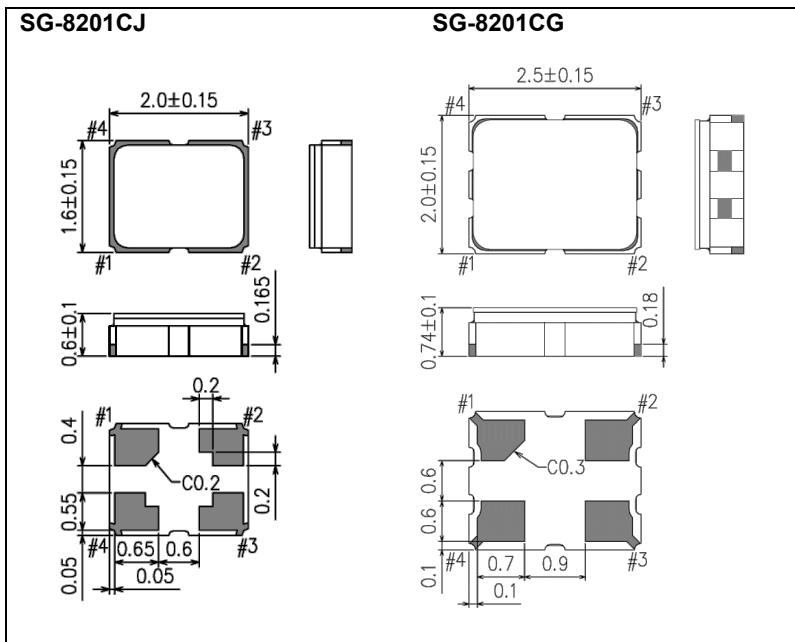
h: Rise/Fall time	
A	Default
B	Faster
C	Fast
D	Slow
E	Slower

External dimensions

(Unit: mm)

Footprint (Recommended)





(Unit: mm)



Notes:

In order to achieve optimum jitter performance, the 0.1 μF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

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	<p>► Pb free.</p>
	<p>► Complies with EU RoHS directive. *About the products without the Pb-free mark. Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)</p>
	<p>► Designed for automotive general equipment.</p>
	<p>► Designed for automotive applications related to driving and safety.</p>

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